WHAT IS CLAIMED IS:

1. A method for detecting baudrate in a Universal Asynchronous Receiver/Transmitter (UART), comprising:

calculating a first number of samplings for each pulse width based on at least one pulse generated from received data;

determining an estimated baudrate and a second number of samplings corresponding to the estimated baudrate based on the first number of samplings for each pulse width, respectively; and

detecting an optimum baudrate based on the second number of samplings.

2. The method of claim 1, wherein calculating a first number of samplings for each pulse width is conducted by using at least one prescribed baudrate.

3. The method of claim 1, wherein the estimated baudrate and the second number of samplings corresponding to the estimate baudrate are determined when the first number of samplings of a first input pulse width among a plurality of pulse widths is less than or equal to a prescribed value.

4. The method of claim 3, wherein the prescribed value is 10.

5. The method of claim 3, wherein the second number of samplings is adjusted by a prescribed baudrate in a descending order from a maximum baudrate until the second number of samplings becomes less than or equal to the prescribed value, if the first number of samplings of the first input pulse width is greater than the prescribed value.

6. The method of claim 5, wherein the prescribed value is 10.

7. The method of claim 1, wherein calculating the estimated baudrate is executed by employing a mapping table.

8. The method of claim 1, wherein at least two estimated baudrates are calculated.

9. The method of claim 1, wherein detecting the optimum baudrate comprises:

providing the second number of samplings calculated based on the first number of samplings of a first pulse width by means of a baudrate detector corresponding to the estimated baudrate;

adding a present and a next sampling number in the baudrate detector until the number provided becomes greater than a prescribed number; and

storing word bits or removing word bits previously stored depending on the number of pulse widths and whether an error has occurred, if the sampling number exceeds the prescribed number.

10. The method of claim 9, wherein the prescribed number is 10.

11. The method of claim 9, further comprising generating an active signal in storing the word bits and determining whether the optimum baudrate was detected by calculating the number of a active signal.

12. An apparatus for detecting a baudrate in a Universal Asynchronous Receiver/Transmitter, comprising:

means for calculating a number of samplings for each of at least one pulse width based on at least one pulse produced from received data;

means for determining an estimated baudrate and a second number of samplings corresponding to the estimated baudrate, respectively, based on the first number of samplings for each pulse width; and

means for adding together a present and a next sampling number until the second number of samplings corresponding to the estimated baudrate becomes greater than a prescribed number, and outputting word bits depending on the number of pulse widths and whether an error has occurred.

13. The apparatus of claim 12, wherein the prescribed number is 10.

14. The apparatus of claim 12, wherein the means of adding and outputting comprises a 1X baudrate detector, a 1.5X baudrate detector, a 2X baudrate detector, a 3X baudrate detector, a 4X baudrate detector, a 6X baudrate detector, and a 8X baudrate detector.

15. The apparatus of claim 14, wherein the 1X, 1.5X, 2X, 3X, 4X, 6X, and 8X baudrate detectors generate active signals when the respective word bit is output, respectively.

16. The apparatus of claim 15, further comprising:

means for storing the word bits; and

means for determining whether an optimum baudrate was detected by the number of active signals generated from 1X, 1.5X, 2X, 3X, 4X, 6X, and 8X baudrate detectors.

17. The apparatus of claim 12, further comprising means for inputting/outputting the respective pulse width calculated by the means for determining according to a first in first out (FIFO) sequence.

18. The apparatus of claim 13, wherein the means for calculating adjusts the number of samplings of pulse width in accordance with a prescribed baudrate.

19. The apparatus of claim 13, wherein the means for determining the estimated baudrate calculates the estimated baudrate and the second number of samplings corresponding to the estimated baudrate by utilizing a mapping table.

20. The apparatus of claim 13, wherein the means for determining the estimated baudrate calculates the estimated baudrate when the number of samplings of the first input pulse width among the number of samplings of a plurality of pulse widths becomes less than or equal to the prescribed number.

21. The apparatus of claim 13, wherein the available baudrate means activates only the X baudrate detector corresponding to a second estimated baudrate when a first estimated baudrate is not equal to the second estimated baudrate, wherein the first estimated baudrate is the baudrate calculated from a previous pulse width and the second estimated baudrate is the baudrate calculated from a next pulse width.

22. A baudrate detection device, comprising:

a pulse generator, configured to receive an input signal and generate at least one pulse;

a sampling calculator, coupled to receive an output of the pulse generator and configured to generate a first sampling number for the least one pulse in accordance with an estimated baudrate;

an estimated baudrate detector, coupled to receive the first sampling number and determine the estimated baudrate and a second sampling number; and

an optimum baudrate detector unit, configured to generate an optimal baudrate in accordance with the estimated baudrate and the second sampling number.

23. The device of claim 22, further comprising a register coupled to receive an output of the sampling calculator, configured to store the first sampling number and provide the first sampling number to the estimated baudrate detector.

24. The device of claim 22, wherein the estimated baudrate detector comprises a table to map the first sampling number to the estimated baudrate and the second sampling number.

25. The device of claim 22, further comprising a buffer configured to store an output of the optimum baudrate detector unit.

26. The device of claim 22, further comprising a counter configured to count an output of the optimum baudrate detector unit.

27. The device of claim 22, wherein the optimum baudrate detector unit comprises a plurality of optimum baudrate detectors, each configured to detect a prescribed baudrate.